PROCESS FOR TRANSFERRING A LAYER OF
STRAINED SEMICONDUCTOR MATERIAL

FIELD OF THE INVENTION

The present invention relates to the transfer of a thin layer of a donor wafer to a receiving substrate in order to form structures such as a semiconductor-on-insulator structure. The invention is aimed more particularly at carrying out this transfer in order to produce electronic structures comprising strained layers.

BACKGROUND OF THE INVENTION

Several processes and techniques for transferring semiconductor layers, such as Si or SiGe layers, have been proposed, in which the donor wafer comprises in succession a single-crystal silicon support substrate and a thickness of SiGe. Zhi-Yuan Cheng et al. of Massachusetts Institute of Technology has presented, in a document entitled *"SiGe-On-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility Evaluation"* (2001 IEEE International SOI Conference, 10/01), two known techniques for transferring layers applied to the donor wafer including a SiGe buffer layer.

The first of these layer transfer techniques is called "etch-back". It consists of removing, by chemical-mechanical means, the single-crystal Si support substrate and the SiGe buffer layer after bonding the donor wafer to the receiving substrate. In particular, an etching called "selective etching" is used to remove the buffer layer, as this has the ability of etching the strained SiGe of the buffer layer more easily than the relaxed SiGe of the surface layer. The relaxed SiGe layer then behaves as a "stop layer" for the etching, since the etching stops at least partly at the level thereof.

Finally, a strained Si film is then grown epitaxially on the relaxed SiGe layer in order to produce a strained Si-on-SiGe structure. In this final structure, a layer of relaxed material (in this case, the layer of SiGe) is interposed between the layer of strained material (in this case the Si film) and the oxide.

This may substantially reduce the technical performance expected of the Si/SiGe combination, and especially its electrical properties. Thus, for example, the SiGe layer may have a tendency to increase the circuit capacitances and therefore reduce the

switching rates of the electronic components to be produced or produced in the Si/SiGe active part.

The fabrication of electronic components in the active part of such a structure comprising this combination having two on-insulator layers also has the risk of being complex to carry out, especially by the creation of lateral insulating regions in the on-insulator combination. This process furthermore limits the application to the production of an Si/SiGe-on-insulator structure and provides no solution to the production, for example, of a strained Si-on-insulator structure.

Other etch-back techniques and processes have also been proposed, for example, in U.S. Patent No. 5,013,681, in which an unstrained Si layer is especially transferred;

The second layer transfer technique reported in the document by Zhi-Yuan Cheng et al. is based on the "SmartCut®" technology of Soitec S.A., which is known to those skilled in the art, and descriptions of which may be found in a number of works dealing with wafer reduction techniques. In the SmartCut® process, before bonding, an ion species is implanted into the relaxed SiGe layer to create a region of weakness therein. After bonding, the donor wafer splits or is cut at the region of weakness. What is obtained therefore is, on the one hand, a donor wafer, stripped of part of the relaxed SiGe layer, and, on the other hand, a structure comprising, bonded together, a removed thin layer of relaxed SiGe and the receiving substrate. The SmartCut® technique is advantageous in that it affords the possibility of recycling the donor wafer instead of sacrificing it, unlike the etch-back technique.

Other processes have been proposed, using the two techniques simultaneously. U.S. Patent No. 5,882,987 and a document by K.D. Hobart et al. from the Naval Research Laboratory in Washington ("*On scaling the thin film Si thickness of SOI substrates*") disclose an overall process for producing a "semiconductor-on-insulator" (also called SeOI) structures from a donor wafer comprising in succession a single-crystal Si base support substrate, an SiGe layer and an epitaxially grown Si film bonded to an oxidized support substrate. In these disclosures, the SmartCut® technique is employed, creating, before bonding, a region of weakness in the Si support substrate which, after bonding, causes detachment in the donor

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wafer in this region. A structure consisting in succession of part of the Si support substrate, the SiGe layer and the epitaxially grown Si film is thus removed, the whole assembly being bonded to the oxidized receiving substrate.

Two successive selective etching operations are then carried out on the structure firstly to remove the remaining part of the Si support substrate with an etching solution, such that the SiGe layer forms a stop layer, and then to remove the SiGe layer with an etching solution such that the Si film forms a stop layer. The resulting structure is an SeOI structure with a surface Si layer. This silicon layer is both very thin and very uniform through its thickness, and is provided using a process which can avoid a finishing step which would otherwise be prejudicial to the quality of the silicon layer. The main objective of this process is not, however, to produce an SeOI structure with a strained silicon layer. The SiGe layer used to produce the SeOI structure during implementation of this process has a typical thickness of between 0.01 and 0.2 microns, a thickness insufficient to fulfill the role of a buffer layer between the Si support substrate and a potential relaxed SiGe layer. The silicon of the film grown epitaxially on the SiGe layer and constituting the Si layer of the final SeOI structure therefore would be little strained or unstrained, and therefore does not achieve production of a structure comprising a strained Si layer so as to benefit from its useful electrical properties, especially in SeOI structures. Also, since the instruments for implanting species are very often limited to about 200 keV, the associated maximum implantation depths would correspond substantially to the minimum thickness of a reliable buffer layer, i.e., about one to two microns, which is insufficient to implant into the Si support substrate, so it would be difficult to use this process with an SiGe layer thick enough to contain both a buffer layer and a relaxed surface SiGe layer. More powerful implantation instruments require am equipment infrastructure that would be very expensive and the operating costs could be prohibitive. This type of process therefore seems to be unsuitable for producing a structure comprising a strained Si layer.

An IBM document by L.J. Huang et al. ("*SiGe-On-Insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors*", Applied Physics Letters, 26/02/2001, Vol. 78, No. 9), discloses for example a process for producing an Si/SGOI structure with strained silicon, starting from a donor wafer comprising in succession a single-crystal Si support substrate, a SiGe buffer layer and a relaxed SiGe layer.

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The process employed consists in using the SmartCut® technique in the relaxed SiGe layer, thus making it possible, after bonding to an oxidized receiving substrate and after cutting in the region of weakness created beforehand, to produce a SGOI structure with relaxed SiGe. A film of strained Si is then epitaxially grown on the relaxed SiGe layer in order to produce a Si/SGOI structure. In this final structure, a layer of relaxed material (i.e., the SiGe layer) is subjacent to the layer of strained material (i.e., the Si film). This may be prejudicial to the performance, especially the electronic performance, expected in this case of the layer of strained material, as already mentioned above. This process furthermore limits the application to the production of such a Si/SiGe-on-insulator structure and does not provide a solution to the production, for example, of a strained Si-on-insulator structure.

PCT Publication WO 01/99169 discloses processes for producing, from a wafer consisting in succession of a Si substrate, a SiGe buffer layer, a relaxed SiGe layer and, optionally, a layer of strained Si or SiGe, a final structure having the relaxed SiGe layer on the optional other strained Si or SiGe layer. The technique employed to produce such a structure involves, after bonding the wafer to a receiving substrate, removal of material from the wafer that it is not desired to retain, by selectively etching the Si substrate and the SiGe buffer layer. This technique does make it possible to achieve thin layer thicknesses having homogeneity through the thickness, but it does entail, however, the destruction of the Si substrate and of the SiGe buffer layer by chemical etching. These processes do not therefore afford the possibility of reusing part of the wafer, and especially at least part of the buffer layer, for a new layer transfer. Moreover, these processes do not provide a solution to the production of a simple strained silicon-on-insulator structure.

Accordingly, there is a need for a process to produce strained silicon-on-insulator which can overcome the above drawbacks.

SUMMARY OF THE INVENTION

The invention relates to a semiconductor wafer and a method of preparing a semiconductor wafer with a strained layer, which may have improved electrical properties. In a preferred embodiment of the method, a region of weakness configured to facilitate splitting is created in a matching layer that has a first lattice parameter. The region of weakness can be created, for example, implanting atomic species or by adding a porous layer. A strained layer

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of a semiconductor material is grown on the matching layer in a strained state to impart the same first lattice parameter in the strained layer as in the matching layer. A receiving substrate is associated with the strained layer to form a composite structure. Product and donor wafers are obtained by splitting the composite structure at the region of weakness. The product wafer includes the strained layer and the receiving substrate, and the donor wafer includes at least a portion of the matching layer.

The matching layer is preferably grown on a handling substrate that has a second lattice parameter that is different from the first lattice parameter, and the matching layer can include a buffer layer that is graded between the first and second lattice parameters, preferably such that the surface of the matching layer on which the strained layer is grown is substantially relaxed. Advantageously, the lattice parameter of the first material when strained is different than the lattice parameter of the first material in a relaxed state.

The receiving substrate is preferably bonded to the strained layer. Also, the strained layer is preferably disposed directly adjacent an insulator on a side of the strained layer on which the receiving substrate is disposed, and an insulator layer can be provided between the strained layer and receiving substrate. A portion of the matching layer can be retained on the strained layer after splitting. Additionally, a step to smooth roughness from the retained portion may be conducted, or the retained portion may be selectively etched from the strained layer.

The preferred material for the strained layer is Si, and for the matching layer is SiGe. Additionally, the region of weakness is preferably formed prior to growing the strained layer.

In the preferred embodiment, the strain imparted to the strained layer is sufficient for modifying the energy band structure of the strained layer material for improving the electrical properties thereof compared to the material in a relaxed state. The strained layer has a thickness that is sufficiently thin to prevent substantial relaxation of the strain. This thickness is preferably less than about 20 nanometers. The resulting charge carrier mobility in the strained semiconductor material layer is at least about 50% higher than in the same semiconductor material in a relaxed state.

In one embodiment, a strain-retaining layer having the first lattice parameter can be provided on the strained layer in association therewith for maintaining the strain from

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the side of the strained layer opposite the receiving substrate. The matching and strain-retaining layers can be made of substantially the same material.

In another embodiment, a second strained layer of a semiconductor material is provided on the first strain-retaining layer to impart the first lattice parameter therein. This enables the second strained layer to be transferred to a second receiving substrate after creating a weakened region in the first strain-retaining layer, and the first strained layer to be transferred to a first receiving substrate, such as after the transfer of the second strained layer. A second strain-retaining layer can be provided on the second strained layer substantially with the first lattice parameter for maintaining the strained state of the second strained layer from the side of the second strained layer opposite the first strain-retaining layer.

The second receiving substrate can be associated with the strained layers to form a second composite structure, and a second product wafer and a second donor wafer can be obtained by splitting the second composite structure at the second region of weakness. Preferably, the second product wafer includes the second strained layer and the second receiving substrate, while the second donor wafer includes at least a portion of the first strain-retaining layer. The first region of weakness can be created in the first strain-retaining layer, and the first receiving substrate can be associated with the second donor wafer to form the first composite structure. In this embodiment, a first product wafer and first donor wafer are obtained by splitting the first composite structure at the first region of weakness. The first product wafer preferably includes the first strained layer and the first receiving substrate, while the first donor wafer includes at least a portion of the matching layer.

A semiconductor wafer of a preferred embodiment of the invention includes a matching layer having a first lattice parameter and a strained layer of a semiconductor material grown on the matching layer in a strained state to impart the same first lattice parameter in the strained layer as in the matching layer. The wafer also has a strain-retaining layer grown on the strained layer in a substantially relaxed state and having the same first lattice parameter for maintaining the strained state of the strained layer from the side of the strained layer opposite the receiving substrate.

In one embodiment, a second strained layer is disposed on the first strain-retaining layer and is strained to impart the first lattice parameter therein. A second strain-retaining layer is on the second strained layer in a substantially relaxed state and has the first

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lattice parameter for maintaining the strained state of the second strained layer from the side of the second strained layer opposite the first strain-retaining layer.

A repeating pattern of first and second layers can be provided, such as on the matching layer. This preferably allows for performing multiple transfers of a portions of the pattern to a receiving substrate to produce product wafers, with each portion including at least one of the first layers.

An oxide of the material of the first strained layer can be bonded thereto as the strain retaining member before splitting. Preferably, the first strained layer comprises silicon, and the method further comprising bonding silica to the silicon of the first strained layer prior to splitting. Additionally, the transferred strained layer of portion thereof remaining thereof can be thickened epitaxially to produce a thicker strained layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Further aspects and advantages of the present invention will be more clearly apparent on reading the following detailed description of the implementation of preferred processes thereof, these being given by way of non-limiting example and with reference to the appended drawings, in which:

Figs. 1a-d show various steps of a first process for producing an electronic structure comprising a thin layer of strained silicon according to the invention;

Figs. 2a-d show various steps of a second process for producing an electronic structure comprising a thin layer of strained silicon according to the invention;

Figs. 3a-e show various steps of a third process for producing an electronic structure comprising a thin layer made of strained silicon according to the invention;

Figs. 4a-e show various steps of a fourth process for producing an electronic structure comprising a thin layer of strained silicon according to the invention;

Figs. 5a-g show various steps of a fifth process for producing an electronic structure from a stack of strained semiconductor layers; and

Figs. 6a-c show various steps of a sixth process for producing an electronic structure from a stack of strained semiconductor layers.

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DETAILED DESCRIPTION FO THE PREFERRED EMBODIMENTS

The expression "strained layer" is understood here to mean any layer of a semiconductor material with a crystallographic structure that is strained in tension or in compression during crystal growth, such as during epitaxy, with at least one lattice parameter that is substantially different from the nominal lattice parameter of this material. Conversely, the term "relaxed layer" means any layer of a semiconductor material which has an unstrained crystallographic structure. That is to say, one which has a lattice parameter substantially identical to the nominal lattice parameter of the material of the layer.

The invention aims to produce an SeOI structure. The strain exerted within the semiconductor material of the produced SeOI may in fact exhibit physical and/or electrical properties worthwhile exploiting. Thus, for example, a main benefit of tension-strained silicon layers (also called strained Si layers) consists mainly in the fact that the charge carriers (such as holes and electrons) have a higher mobility than that usually found in relaxed Si layers. The strained Si layers may in this regard reach a charge carrier mobility 100% higher than that within relaxed Si layers, and preferably the charge carrier mobility is at least about 50% higher.

To produce such strained Si layers, it is known to grow a silicon film by epitaxy on a base composed of silicon and germanium. Since germanium in equilibrium has a lattice parameter slightly greater than that of the silicon in equilibrium (greater by approximately 4%), the presence of germanium in a defined amount in the silicon thus makes it possible to slightly increase the lattice parameter compared with a base consisting only of silicon. This silicon-germanium base (also called SiGe base) will thus strain the epitaxially grown Si film so as to make its lattice parameter substantially identical to its own.

In practice, a substrate made of bulk SiGe is not available on the market and the SiGe base is then generally composed of a single-crystal Si support substrate on which a relaxed SiGe layer is produced via a buffer layer. The term "buffer layer" is understood to mean an intermediate layer between two crystallographic structures with different lattice parameters, having in the region of one of its faces a lattice parameter substantially identical to that of the first structure and in the region of its other face a lattice parameter substantially identical to that of the second structure. The buffer layer inserted between the Si support substrate and the relaxed SiGe layer is generally made of SiGe, with a quantity-wise

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proportion of germanium which progressively increases through the thickness of the support substrate towards the relaxed layer.

Thus, the buffer layer has a thickness sufficient to make it possible to:

- to gradually increase the germanium content from the support substrate towards the relaxed layer;

- to confine defects associated with the difference in lattice parameter so that they are buried; and

- to give a sufficiently thick relaxed SiGe layer stability with respect to an Si film grown epitaxially on its surface in order to strain the latter so as to modify its lattice parameter without influencing that of the relaxed SiGe layer. The thickness of the buffer layer is preferably about between one and three microns.

In the field of application of the present invention, this type of wafer is used as a donor in the sense that at least a layer of material is removed therefrom in order to transfer it to a receiving substrate. This transfer generally comprises a first step of bonding the donor wafer to the receiving substrate. A second step consists in keeping of the bonded donor wafer only at least one thin layer adjacent to the bonding region, by removing the superfluous parts from the donor wafer.

The preferred process of the invention for producing an electronic structure comprising a thin layer of strained semiconductor material from a donor wafer comprising a lattice parameter matching layer comprising an upper layer of semiconductor material having a first lattice parameter, includes the following steps:

(a) growth of a film of semiconductor material on the upper layer of the matching layer, which film has a second, nominal, lattice parameter substantially different from the first lattice parameter, with a thickness small enough to keep the first lattice parameter of the upper layer of the subjacent matching layer and thus to be strained;

(b) formation of a region of weakness in the wafer on the matching layer side in relation to the film, the location of which in each of the following embodiments is shown at 7 in Figs. 1c, 2c, 3d, and 4d;

(c) bonding of a receiving substrate with the donor wafer on the film side; and

(d) removal of at least part of the donor wafer on the matching layer side in relation to the film, comprising supply of energy into the region of weakness in order to detach a structure which includes the relaxed layer from the wafer.

Additionally, embodiments of the invention include the following aspects:

- in step (d) relates substantially the entire portion of the donor wafer disposed on the same side of the film as the matching layer can be removed;

- step (d) can be carried out so as not to remove part of the donor wafer on the side of the film where the matching-layer is disposed, and this unremoved portion can include part of the matching layer close to the film. In this case, a process for correcting the surface roughness may be carried out on the surface of the unremoved portion of the matching layer;

- after step (a), a step of growing at least one growth layer on the film can additionally be carried out, and preferably the growth layer does not substantially decrease the strained state of the film. In the latter case, the growth layer preferably has a nominal lattice parameter substantially identical to the first lattice parameter;

- after step (a), steps of growing, on the film, layers not substantially decreasing the strained state of the film can be carried out. These growth layers preferably form a multilayer structure having a layer having the first lattice parameter and a strained layer made of semiconductor material having a nominal lattice parameter substantially different from the first lattice parameter. The growth layer directly adjacent to the film is preferably a layer having the first lattice parameter;

- between step (a) and step (c), a step of forming at least one bonding layer between the receiving substrate and the donor wafer can be additionally carried out, with the bonding layer formed on the receiving substrate and/or on the bonding face of the donor wafer. The bonding layer can be made of silica;

- the bonding may carried out by molecular adhesion (wafer bonding);

- the bonding is preferably accompanied by a heat treatment in order to strengthen the bonds;

- the region of weakness is preferably formed by implantation of atomic species into the matching layer at a depth substantially equal to the implant depth;

- before step (a), the region of weakness can be formed by porosification of a layer beneath the film;

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- step (d) can comprise, after the energy supply operation of step (d), an operation of selectively etching the material having the first lattice parameter with respect to the material constituting the film in order to remove the remainder of the matching layer;

- the preferred film of strained material is made of silicon and the preferred matching layer is made of silicon-germanium, the matching layer comprising a buffer layer with a germanium concentration that increases through the thickness and the upper layer which is relaxed beneath the strained film. If part of the matching layer remains after removal during step (c), this part of the matching layer is preferably at least part of the upper relaxed silicon-germanium layer of the matching layer;

- in either of the two immediately preceding cases, and if a growth layer has been grown on the film, this growth layer is preferably made of relaxed silicon-germanium, with a germanium concentration substantially equal to the germanium concentration of the relaxed upper layer of the matching layer;

- the receiving substrate can be made of silicon;

- the wafer preferably comprises at least one layer furthermore containing carbon, with a carbon concentration in the layer substantially less than or equal to 50%; and

- the wafer (10) preferably comprises at least one layer furthermore containing carbon, with a carbon concentration in the layer substantially less than or equal to 5%.

The invention provides semiconductor-on-substrate structures, which can be produced in accordance with the above process. Preferably, the thickness of semiconductor of the structure includes:

- the film; or

- part of the matching layer on the film; or

- the film on the growth layer having a nominal lattice parameter substantially identical to the first lattice parameter; or

- the film on a multilayer structure; or

- part of the matching layer on the film on the growth layer having a nominal lattice parameter substantially identical to the first lattice parameter; or

- part of the matching layer on the film on a multilayer structure;

- and there is a layer of electrically insulating material beneath the thickness of the semiconductor of the structure, so that the structure is a semiconductor-on-insulator structure.

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The present invention provides a reliable process for transferring a film of strained material from a donor wafer to a receiving substrate, the assembly then forming the desired electronic structure, without relaxing the strain within the film during transfer. An example of a process according to the invention will now be described below with reference to Figs. 1a, 2a, 3a and 4a from a donor wafer 10 consisting in the first place of a single-crystal silicon support substrate 1 and an SiGe lattice parameter matching layer 2. The expression "lattice parameter matching layer" denotes any structure behaving as a buffer layer. In the preferred embodiment, the matching layer has, on the surface, a layer of substantially relaxed material without an appreciable number of structural defects, such as dislocations.

Thus, in our example, it will be advantageous to choose an SiGe matching layer 2 consisting in succession of a SiGe buffer layer and a relaxed SiGe layer on the surface. The buffer layer preferably has a germanium concentration which grows uniformly from the interface with the support substrate 1, for reasons which were explained above. Its thickness is typically between 1 and 3 micrometers in order to obtain good structural relaxation on the surface. The relaxed SiGe layer has advantageously been formed by epitaxy on the surface of the buffer layer and its thickness may vary widely depending on the case, with a typical thickness of between 0.5 and 1 micron.

The germanium concentration in the silicon within the relaxed SiGe layer is typically about between 15% and 30% in order to obtain, during the next step (shown by Figs. 1b, 2b, 3b or 4b), an epitaxially grown Si film 3 sufficiently strained in order to have appreciable electrical properties and not too strained so as to prevent internal structural defects from appearing. This 30% upper end represents a typical maximum used in the current techniques, but this upper end may increase in the coming years and in other processes.

With reference to FIGS. 1b, 2b, 3b and 4b, an Si film 3 is grown on the SiGe matching layer 2. The Si film 3 is advantageously formed by epitaxy using known techniques such as CVD (chemical vapour deposition) and MBE (molecular beam epitaxy) techniques. The silicon lying within the film 3 is then obliged by the matching layer 2 to increase its nominal lattice parameter in order to make it substantially identical to that of its growth substrate and thus introduce internal tensile strains.

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These modifications of its internal crystallographic structure will increase the mobility of the charge carriers (such as holes and electrons) by modifying the energy band structure of the silicon crystal. The electrical properties desired in this invention are thus obtained. It is desired, however, to form quite a thin Si film 3, as too great a film thickness could cause at least partial relaxation of the strain in the thickness of the film towards the nominal lattice parameter of the silicon. The thickness of the film 3 is thus typically less than about 20 nanometers, and preferably about between 10 and 20 nanometers. Above about 20 nanometers there is a risk of substantial relaxation of the strain that is desired in the present invention, and below about 10 nanometers there is a risk of the thickness of the film causing problems in the fabrication of certain electronic components.

Once this donor wafer 10 containing a strained Si film 3 has been produced, one difficulty resides in implementing a reliable process for transferring the strained film 3 from the donor wafer 10 onto a receiving substrate 4, the whole assembly then forming the desired electronic structure 20 without any relaxation of the strain within the film 3 during transfer. To solve this particular difficulty, several methods of implementation may be suggested.

In a first method of implementing the process according to the invention, with reference to FIGS. 1c and 2c, a receiving substrate 4 is attached to the surface of the strained film 3. This receiving substrate 4 may, for example, be made of silicon or may consist of other types of material. The receiving substrate 4 is attached by bringing it into intimate contact with the strained Si film 3 and carrying out bonding, in which molecular adhesion between the substrate 4 and the film 3 is advantageously effected. This bonding technique, as well as variants, is for example described in the document entitled *"Semiconductor Wafer Bonding"* (Science and Technology, Interscience Technology) by Q.Y. Tong, U. Gösele and Wiley.

If necessary, bonding is accompanied by an appropriate prior treatment of the respective surfaces to be bonded and/or by supplying thermal energy and/or supplying an additional tie layer. Thus, for example, a heat treatment carried out during bonding allows the bonds to be strengthened.

Bonding may also be reinforced by a bonding layer inserted between the film 3 and the receiving substrate 4, which makes it possible to produce molecular bonds both with

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the film 3 and with the material constituting the bonding face of the receiving substrate 4 which are stronger than those existing between the film 3 and the receiving substrate 4.

Silicon oxide (also called silica or SiO_2) is a material that may be chosen for producing such a bonding layer, as it exhibits good adhesion with the silicon of the film 3. The silica may be formed on the film 3 and/or on the receiving substrate 4 by SiO_2 deposition or by thermal oxidation on the respective bonding surfaces.

Preferably, the material constituting the bonding face of the receiving substrate 4 and/or the material of the bonding layer optionally formed is electrically insulating, so that there exists an insulating layer directly adjacent to the strained Si film 3. A conducting or semiconducting material directly adjacent to the film 3 could impair the electrical effects desired here in a structure consisting of the combination of the two materials. This advantageous choice of insulating material adjacent to the film 3 becomes particularly useful when the structure 20 that it is desired to produce in the end is an SeOI structure, the semiconductor layer of the SeOI structure then being the transferred film 3 of strained Si. Moreover, the receiving substrate 4 bonded to the strained Si film 3 makes it possible to retain substantially the strained structural state of the strained Si of the film 3, this being so even if the donor wafer 10 on which the strained Si film 3 has been grown epitaxially is removed, the strain within the film 3 being mainly ensured after transfer by the bonding forces existing between the film 3 and the receiving substrate 4.

Transfer of the strained film 3 from the donor wafer 10 to the receiving substrate 4 without relaxing the strain within the film 3 is thus made possible, thereby solving the abovementioned difficulty.

The receiving substrate 4 preferably provides mechanical support sufficiently rigid to sustain the strained Si film 3 and protect it from any mechanical stresses coming from the outside. Once the receiving substrate 4 has been bonded, part of the donor wafer 10 is removed using one or more of the preferred techniques that will be explained later, in order to transfer the strained Si film 3 to the receiving substrate and to produce the desired structure 20.

In a first case, with reference to FIG. 1d, substantially all that part of the donor wafer 10 on the matching layer 2 side in relation to the strained film 3 is removed. Thus, a final strained Si-on-substrate structure, and in particular a strained Si-on-insulator structure

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(also called here an SOI structure), is obtained if the material subjacent to the strained Si film 3 is an electrical insulator.

In a second case, with reference to FIG. 2d, the support substrate 1 and part of the matching layer 2 are removed. Thus, a final SiGe-on-strained Si-on-substrate structure, and in particular an SiGe-on-strained Si-on-insulator structure (also called SiGe/SOI structure), is obtained if the material subjacent to the strained Si film 3 is an electrical insulator. The removal of part of the matching layer 2 is advantageously carried out so as to preserve of the matching layer 2 on the structure 20 only at least part of the relaxed SiGe layer present in the matching layer 2 (and which had been epitaxially grown according to one particular method of producing the matching layer 2 explained above, on a buffer layer).

According to a second method of implementing the process according to the invention, with reference to FIGS. 3c and 4c, a relaxed SiGe layer 6 is grown on the strained Si film 3, by epitaxy (for example by CVD or MBE) advantageously before any bonding operation. The Ge concentration in this layer 6 is advantageously and substantially the same as that of the SiGe present near the bonding face of the matching layer 2 so as to prevent this layer having an additional influence on the strain in the film 3.

In one particular method of implementation, further layers may be grown epitaxially on the SiGe layer, such as strained Si or SiC layers and SiGe or SiGeC layers respectively alternating in order to form a multilayer structure.

Referring to FIGS. 3d and 4d, a receiving substrate 4 is bonded to the relaxed SiGe layer 6 in a manner substantially identical to that explained above in the first method of implementation and relating to a receiving substrate 4 bonded to the strained film 3. The bonding face of the donor wafer 10 is then the free face of the relaxed SiGe layer 6.

It should be pointed out that, unlike the first method of implementation, the bonds do not necessarily constitute the only means of preserving the strain in the film 3. This is because if the relaxed SiGe layer 6 is thick enough, it may participate in or even cause the preservation of the strain in the film 3 after these two layers have been transferred. The thickness of the SiGe epilayer 6 may thus be judiciously chosen in this regard so as to preserve greater or lesser amounts of the strain in the Si layer.

As in the first method of implementation, once the receiving substrate 4 has bonded, part of the donor wafer 10 is removed using one or more of the preferred techniques

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that will be explained below, in order to transfer the strained Si film 3 to the receiving substrate 4 and produce the desired structure 20. In a first case, with reference to FIG. 3e, all that part of the donor wafer 10 on the matching layer 2 side in relation to the layer 6 is removed. Thus, a final strained Si-on-relaxed SiGe-on-substrate structure, and in particular a strained Si-on-relaxed SiGe-on-insulator structure (also called an Si/SGOI structure), is obtained if the material subjacent to the relaxed SiGe layer 6 is an electrical insulator.

In a second case, with reference to FIG. 4e, the Si support substrate 1 and part of the matching layer 2 are removed. Thus, a final SiGe-on-strained Si-on-relaxed SiGe-on-substrate structure, and in particular an SiGe-on-strained Si-on-relaxed SiGe-on-insulator structure (also called an SiGe/Si/SGOI structure), is obtained if the material subjacent to the relaxed SiGe layer 6 is an electrical insulator. Part of the matching layer 2 is advantageously removed so as to preserve of the matching layer 2 on the structure 20 only at least part of the relaxed SiGe layer present in the matching layer 2 (and which had been epitaxially grown, using one particular method of producing the matching layer 2 explained above, on a buffer layer).

Thus, by means of the process according to the invention several structures (shown for example in FIGS. 1d, 2d, 3e and 4e) comprising a layer of strained material can be produced, each having very specific electrical properties.

With reference to FIGS. 1d, 2d, 3e and 4e, removal of material constitutes the final step of producing such structures. A first material removal operation consists in cutting the donor wafer in a region of the matching layer 2 that has previously been weakened therein. The techniques for perform such an operation include the following two known techniques.

A first technique, called the SmartCut® technique, known to those skilled in the art (and descriptions of which may be found in a number of works dealing with wafer reduction techniques), consists in implanting atomic species (such as hydrogen ions) and then in subjecting the implanted region, which then forms a region of weakness, to a heat treatment and/or mechanical treatment, or another supply of energy, in order to make the cut in the region of weakness. Cutting a region of weakness thus formed in the matching layer 2 makes it possible to remove most of the wafer 10, in order to obtain a structure comprising

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the remainder of the matching layer 2, the strained Si film 3, optionally epitaxially grown overlayers such as the layer 6, the optional bonding layer and the receiving substrate 4.

A second technique consists in obtaining a weak interface by creating at least one porous layer, as described for example in document EP-A-0 849 788, and then in subjecting the weak layer to a mechanical treatment, or another supply of energy, in order to make the cut in the weakened layer. The weakened layer made of porous silicon is formed within the support substrate 1, between the support substrate 1 and the matching layer 2, in the matching layer 2 (for example between a buffer layer and a relaxed layer) or on the matching layer 2 (that is to say between the matching layer 2 and the strained Si film 3 or the optional relaxed SiGe layer 6).

To form a weakened layer within the support substrate 1, the porous layer is preferably advantageously grown on a single-crystal Si support substrate, and then a second growth is carried out on the porous layer so as to grow a non-porous Si layer having substantially the same lattice parameter as the Si of the support substrate. The support substrate 1 then consists of the support substrate, the porous layer and the non-porous Si layer.

Cutting a weakened layer makes it possible to remove at least some of the wafer 10 to obtain a structure comprising the optional remainder of the wafer 10, the strained Si film 3, optionally epitaxially grown overlayers such as the layer 6, optionally the inserted bonding layer and the receiving substrate 4.

A treatment of the wafer 10, in order to remove the porous silicon which remains after the cutting, is advantageously carried out, such as an etching operation or a heat treatment. If the porous layer lies within the support substrate 1, a lapping, chemical-mechanical polishing and/or selective chemical etching operations are then advantageously carried out in order to remove the remaining part of the support substrate 1.

These two techniques or other suitable techniques make it possible to rapidly remove, en bloc, a substantial part of the wafer 10. They also allow the possibility of reusing the removed part of the wafer 10 in another process, such as for example a process according to the invention.

Thus, if the part removed is the support substrate 1, an operation to reform a matching layer 2, a film 3 and an optional SiGe layer 6 and/or other layers may be carried out

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as described above, after the surface of the support substrate 1 has been polished. If the removed part is the support substrate 1 and at least part of the matching layer 2, a possible reformation of another part of the matching layer 2, of a film 3 and of an SiGe layer 6 and/or other layers may be carried out as described above, after the surface of the remaining part of the matching layer 2 has been polished.

A second material removal operation after cutting the wafer 10 according, for example, to one of the above two techniques can include correcting surface defects or in removing, if necessary, the remaining part of the matching layer 2. If it is desired to remove all of the remaining part of the matching layer 2 (referring to FIGS. 1d and 3e), this operation may be carried out by selective chemical etching so that the strained Si film 3 undergoes little or no etching, thus forming an etching stop layer.

The remaining part of the matching layer 2 is in this case etched by wet etching using etching solutions having a substantial selectivity with respect to the strained Si film 3, such as a solution comprising $HF/H_2O_2/CH_3COOH$ (approximately 1/1000 selectivity) or HNA (hydrofluoric-nitric-acetic solution). Dry etching operations may also be carried out in order to remove material, such as plasma etching, or by sputtering. This chemical method has the main advantage of being quite rapid for thin layers to be removed and of avoiding the use of chemical-mechanical polishing finishing operations usually employed after cutting the wafer.

It thus makes it possible to maintain good surface quality and good thickness homogeneity of the strained Si film 3 obtained during its epitaxy, it preferably having been unnecessary to carry out a mechanical finishing step in the case in which the material removal is completed by a single chemical operation, thus preventing defects from appearing, such as strain-hardened regions, that such a mechanical finishing step is likely to cause. In certain particular cases, gentle polishing is, however, used in order to compensate for any small surface roughnesses.

The chemical etching operation may advantageously be preceded, especially in the case of a thick layer to be removed, by mechanical or chemical-mechanical abrasion by lapping and/or chemical-mechanical polishing CMP of the remaining part of the matching layer 2. If it is desired to maintain part of the matching layer 5 (referring to FIGS. 2d and 4e), it will be advantageous to choose a heat treatment or a polishing, preferably chemical-

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mechanical polishing CMP, in order to remove any roughnesses and thickness homogeneities that might have appeared during cutting of the wafer 10. Etching selectivity with respect to the Ge concentration present in the matching layer 2 (and which increases with the thickness of the matching layer 2) may also be employed, however, the etching slowing down or stopping on the relaxed layer lying within the matching layer 2. Wet etching with a solution comprising TMAH may, for example, be very suitable for carrying out such selective etching, where the relaxed layer of the matching layer 2 has a germanium concentration of about between 20% and 30%. The invention covering other types of techniques as well that are suitable for removing material from a donor wafer 10 in accordance with the process according to the invention.

In one particular embodiment of the structure of the product wafer 20, one or more epitaxial depositions may be carried out on the donor wafer 10, such as epitaxial deposition of an SiGe or SiGeC layer, or epitaxial deposition of a strained Si or SiC layer, or successive epitaxial depositions of SiGe or SiGeC layers and strained Si or SiC layers in alternation, in order to form a multilayer structure.

Having completed the final structure, a finishing step may optionally be carried out, such as finishing treatments, for example like an annealing operation in order to further strengthen the bonding interface between the donor wafer 10 and the receiving substrate 4.

Although the preferred embodiment of the present invention has a SiGe lattice parameter matching layer 2, other embodiments have a matching layer 2 made from other types of type III-V materials or other materials capable of straining the material of the epitaxially overgrown film 3 or another semiconductor material.

Referring to Figs. 5a-g and 6a-c, other embodiments of the invention for producing multiple product wafers are shown. After steps as described with regard to Figs. 4a-4c, a second strained layer 21 of semiconductor material is grown on a first strain-retaining layer 6, as shown in Fig. 5a, to impart the lattice parameter of the strain-retaining layer 6 in the second strained layer 21, which is preferably substantially the same as the lattice parameter of the matching layer 10 and first strained layer 3 in the strained state. A region of weakness 26 can be formed at this stage, as described above, in the first strain-retaining layer 6, such as by implantation through the second strained layer 21.

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In one embodiment, shown in Fig. 5b, a second strain-retaining layer 22 is provided, such as by growing, on the second strained layer 21. The second strain-retaining layer 22 has the first lattice parameter for maintaining the strained state of the second strained layer 21 from the side of the second strained layer 21 opposite the first strain-retaining layer 6. A second receiving substrate 23 is then preferably associated with the strained layers 3,21, such as by bonding the second receiving substrate 23 to the second strain-retaining layer 22.

In another embodiment, which is shown in Fig. 6a, the second receiving substrate 23 is associated with the strained layers 3,21 by bonding directly to the second strained layer 21, as no strain-retaining layer is provided between the second strained layer 21 and the second receiving substrate 23. An insulating layer can also be added at 30, such as by oxidizing the top surface of the one or more of the strained layers 21,3 or by depositing oxides thereon, preferably prior to the association with the receiving substrate 23 or growth of layer 6, respectively. An oxidized layer 30 is shown in Fig. 6a. A similar insulator can be added, for example, between any of the strained layers in the various embodiments of the invention and adjacent layers.

The stack of multiple strained layers interposed with at least one strain-retaining layer permits multiple transfers from different parts of the collective donor wafer. The second strained layer 22 is transferred to the second receiving substrate 23 by splitting at the region of weakness 26 the composite structure 24 thus created into a second product wafer 25 and a second donor wafer 27 by splitting the composite structure 24. The second product wafer 25 in this embodiment includes the second strained layer 21 and the second receiving substrate 23, and the second donor wafer 27 includes at least a portion of the first strain-retaining layer 6. In the embodiment of Figs. 5c-5e, the second strain-retaining layer 22 is part of the second product wafer 25.

A weakened region 7 can be formed in the matching layer 2, which is preferably accomplished at this stage, as shown in Fig. 5d, although it can be accomplished at other points in the process. Referring to Figs. 5f and 6b, a first receiving substrate 4 is associated with the first strained layer 3, either directly or with a strain-retaining layer therebetween. The strain-retaining layer that is therebetween in Fig. 5f can be the remaining portion of the first strain-retaining layer 6 which may be etched or otherwise smoothed. The remaining portion of the strain retaining layer on the second donor wafer 27 can alternatively

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be completely removed, such by etching. The first strained layer 3 is then transferred to the first receiving substrate 4 by splitting the composite structure 28 at the region of weakness 7 to produce a first product wafer 29, including the first strained layer 3 and receiving substrate 4, as shown in Figs. 5g and 6c, and a first donor wafer 10, including at least a portion of the matching layer 2.

In one embodiment, the strained layer is transferred to a layer of an oxide of the strained layer material after the strained layer is transferred to a receiving substrate. After the transfer, preferably any remaining portion of the matching layer is removed from the strained layer, and the transferred strained layer is epitaxially grown to increase its thickness.

Preferably, the strained layer of this embodiment is of silicon and the oxide is silica. When these materials are used, the critical thickness of the strained layer, which is the thickness beyond which the layer relaxes and defects can typically appear in the crystalline structure of the layer, can be significantly increased. This consequently permits a thicker strained layer to be produced than can be produced with the strained silicon being associated directly with silicon germanium. The strained silicon layer can be thickened by growing to achieve a thickness of around 60 nm. Preferably, the strained silicon layer is thickened by growing to a thickness of between about 40 nm and 60 nm.

While illustrative embodiments of the invention are disclosed herein, it will be appreciated that numerous modifications and other embodiments may be devised by those skilled in the art. For example, while in the preferred embodiment a strained silicon film 3 in transferred, other types of films of a semiconductor able to be strained and transferred can be transferred according to a process of the invention. Additionally, in the semiconductor layers, other constituents may be added thereto, such as carbon with a carbon concentration in the layer in question of less than or equal to about 50% or more preferably with a concentration of less than or equal to about 5%. Therefore, it will be understood that the appended claims are intended to cover all such modifications and embodiments that come within the spirit and scope of the present invention.

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